

Atty. Dkt. No. 03CR254/KE (047141-0348)

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) An apparatus that implements services for a waveform application, the apparatus comprising:  
  
an object request broker that marshals data from the waveform application for communication, wherein at least a portion of the object request broker is implemented in hardware; and  
  
an object request broker interface that communicates the marshaled data using a memory pool, wherein at least a portion of the object request broker interface is implemented in hardware and no middleware is used.
2. (Original) The apparatus of claim 1, wherein the apparatus is an application specific integrated circuit (ASIC).
3. (Original) The apparatus of claim 1, wherein the apparatus is a field programmable gate array (FPGA).
4. (Original) The apparatus of claim 1, wherein the object request broker interface comprises a pluggable protocol interface.
5. (Original) The apparatus of claim 1, wherein the object request broker interface comprises a custom interface.
6. (Currently Amended) The apparatus of claim 1, wherein the object request broker is a CORBA (~~Common Object Request Broker Architecture~~) common object request broker architecture broker.

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7. (Original) The apparatus of claim 1, wherein the memory pool comprises a multi-port memory pool.
8. (Original) The apparatus of claim 1, wherein the at least a portion of the object request broker that is implemented in hardware comprises logic and data formatting functions that are determined to consume excessive processor throughput for a software application.
9. (Original) The apparatus of claim 1, wherein the at least a portion of the object request broker interface that is implemented in hardware comprises an operating system protocol stack.
10. (Currently Amended) A method of marshalling transactions for waveform application communications using a ~~CORBA (Common Object Request Broker Architecture)~~ common object request broker architecture broker, the method comprising:
  - marshalling data from a waveform application in a first communication device, wherein at least a portion of the marshalling operation is implemented in hardware; and
  - interfacing the marshaled data with a second communication device using a memory pool, wherein at least a portion of the interfacing operation is implemented in hardware and no middleware is used.
11. (Original) The method of claim 10, wherein the at least a portion of the marshalling operation that is implemented in hardware comprises logic and data formatting functions that are determined to consume excessive processor throughput for a specific software application.
12. (Original) The method of claim 10, wherein the at least a portion of the interfacing operation that is implemented in hardware comprises an operating system protocol stack.

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13. (Original) The method of claim 11, wherein the hardware comprises an application specific integrated circuit (ASIC).
14. (Original) The method of claim 11, wherein the hardware comprises a field programmable gate array (FPGA).
15. (Currently Amended) A system for a joint tactical radio system (JTRS) compliant device that provides communication at low power requirements, the system comprising:
- a hardware-implemented object request broker (ORB) that marshals data from a waveform application;
  - a pluggable protocol interface that communicates the marshaled data from the hardware-implemented ORB, wherein at least a portion of the pluggable protocol interface is implemented in hardware and no middleware is used; and
  - a memory pool that communicates data from the pluggable protocol interface directly and without transport overhead.
16. (Currently Amended) The system of claim 15, wherein the at least a portion of the pluggable protocol interface that is implemented in hardware ~~comprising~~ comprises logic and data formatting functions of the ORB that are determined to consume excessive processor throughput for a specific software application and an interface to a shared memory pool.
17. (Original) The system of claim 16, wherein the hardware comprises an application specific integrated circuit (ASIC).
18. (Original) The system of claim 16, wherein the hardware comprises a field programmable gate array (FPGA).

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19. (Original) The system of claim 15, wherein the JTRS compliant device is in an unmanned craft.

20. (Original) The system of claim 15, wherein the JTRS compliant device is a battery powered radio